REMARKS

This is in response to the Office Action mailed on February 05, 2004. In the Office Action, (i) claims 7, 16, and 37 were objected for being dependent claims; and (ii) claims 1-3, 6, 8-12, 15, 17-36, and 38-39 were rejected under 35 U.S.C. 103(a).

Reexamination and reconsideration of this case is respectfully requested in view of the foregoing amendments and the following remarks.

Claims 1-3, 6-12, and 15-39 were previously pending. Claims 4-5 and 13-14 were previously cancelled without prejudice. No claim has been cancelled by this response. Claims 7, 16, and 37 have been amended. Claims 40-48 have been added. Accordingly, claims 1-3, 6-12, and 15-48 are now at issue. Of those at issue, claims 1, 7, 10, 16, 31, and 37 are independent claims.

Applicant believes that no new matter has been added by this response.

Applicant respectfully thanks the examiner for withdrawing the objections to the Information Disclosure Statements and the specification. Upon receiving a notice of allowance, Applicant will furnish formal drawings that overcome the draftsperson's objections.

I. Information Disclosure Statement

Applicant filed an information disclosure statement on 08/18/2004 coincidentally with the filing of an RCE. Applicant did not receive a checked and signed Form 1449 with the Office Action mailed on 11/18/2004 indicating that the IDS filed on 08/18/2004 was considered.

For its records, Applicant respectfully requests a copy of the checked and signed Form 1449 for the IDS filed on 08/18/2004 with any further action mailed from the USPTO to be sure it has been considered.

II. Claim Interpretation

The Office Action states that in claims 7, 8, 9, the "Examiner hereby interprets 'nominal selected vector measurement' as a basis or reference for calculations." [Office Action, page 8, section 47, lines 1-2].

However, the phrase "nominal selected vector measurement" is no longer used in the claims. See claims 7, 8, and 9 and Applicant's prior response for clarification.

III. Claim Objections

In section 48, the Office Action objected to claims 7, 16, and 37 for being dependent on rejected base claims. The Office Action indicated that these claims would be allowable if rewritten into independent form including all the limitations of the independent claims and the intervening claims.

Applicant has amended claim 7 into independent form by including the limitations of independent claim 1 and dependent claim 6. Applicant has amended claim 16 into independent form by including the limitations of independent claim 10 and dependent claim 15. Applicant has amended claim 37 into independent form by including the limitations of independent claim 31.

Applicant believes that these amendments to claims 7, 16, and 37 now make this objection moot and its withdrawal is respectfully requested.

IV. Claim Rejections 35 U.S.C. 103

In sections 51-115 of the Office Action, claims 1-3, 6, 8-12, 15, 17-36, and 38-39 stand rejected under 35 U.S.C. 103(a) over U.S. Patent No. 5,278,769 issued to Bair et al. ("Bair") in view of U.S. Patent No. 6,601,024 issued to Chonnad et al. ("Chonnad") and in further view of legal precedent (eliminating elements) and "The Computer Science and Engineering Handbook" by Allen B. Tucker, Jr. ("Tucker").

Specifically, claims 1-2, 10-11, 19-23, 25-29, stand rejected under 35 U.S.C. 103(a) over the combination of Bair and Chonnad. Claims 3 and 12 stand rejected under 35 U.S.C. 103(a) over the combination of Bair, Chonnad and legal precedent (eliminating elements). Claims 6, 8-9, 17-18, 24, 30, 31-36, and 38-39 stand rejected under 35 U.S.C. 103(a) over the combination of Bair, Chonnad, and Tucker. [Note that Tucker does not appear to be used in the detailed rejection of claims 2-3 and the related claims 11-12, nor the claims from which they depend, and are thus assumed to stand rejected as recited above.]

Applicant respectfully traverses these 35 USC 103(a) claim rejections of claims 1-3, 6, 8-12, 15, 17-36, and 38-39.

"To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in

the art, to modify the reference or to combine reference
teachings. Second, there must be a reasonable expectation of
success. Finally, the prior art reference (or references when
combined) must teach or suggest all the claim limitations. The
teaching or suggestion to make the claimed combination and the
reasonable expectation of success must both be found in the
prior art, and not based on applicant's disclosure. In re
Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)" [MPEP §
2142; 8th Edition, Rev. 1, Feb. 2003, Pg. 2100-124].

A. Claim Elements are Not Disclosed by Cited References

Applicant respectfully submits that the combination of Bair
and Chonnad and in further view of cited legal precedent and
other cited references do not disclose Applicant's combination
of elements as recited in pending claims 1-3, 6, 8-12, 15, 17-
36, and 38-39.

Applicant's invention as claimed in independent claims 1
and 10 relates to a computer program and method of modifying a
SPICE netlist though use of a template in order to provide
additional circuit analysis involving a perturbing routine where
circuit parameters are periodically altered, a simulation
routine where circuit simulations are run for each circuit
parameter being varied, and an analysis routine to perform a
specified analysis on the results of the circuit simulations.

Regarding independent claim 1, the Office Action alleges
that, Bair discloses:

"adding a first simulation routine to said SPICE netlist
[to perform a reference simulation of said SPICE netlist to
arrive at nominal values for selected vector measurements]" is
disclosed by Bair at Column 3 line 10 "The circuit-level

simulation is run under several different simulated conditions of power supply voltage and temperature characteristics to determine the worst and best case delay characteristics, rise and fall times". Also see column 2 line 52 "SPICE is a "standard simulator" which has grown into a de-facto industry standard over a number of years.. . HSPSCE, and column 4 line 24 "netlist";

"adding a perturbing routine to said SPICE netlist for altering circuit parameter values of said circuit design in a pre-determined manner" is disclosed by Bair at Column 3 line 10 "The circuit-level simulation is run under several different simulated conditions of power supply voltage and temperature characteristics to determine the worst and best case delay characteristics, rise and fall times". Also see column 2 line 52 "SPICE is a "standard simulator" which has grown into a de-facto industry standard over a number of years.. .HSPICE, and column 4 line 24 "netlist";

"adding a second simulation routine to said SPICE netlist for performing simulations of said circuit design for respective altered circuit parameter values to arrive at respective selected vector measurements" is disclosed by Bair at Column 3 line 10 "The circuit-level simulation is run under several different simulated conditions of power supply voltage and temperature characteristics to determine the worst and best case delay characteristics, rise and fall times". Also see column 2 line 52 "SPICE is a "standard simulator" which has grown into a de-facto industry standard over a number of years.. .HSPICE", and column 4 line 24 "netlist"; and

"adding an analysis routine to said SPICE netlist for manipulating at least one of said selected vector measurements

in accordance with said pre-determined analysis" is disclosed by Bair at Column 3 line 10 "The circuit-level simulation is run under several different simulated conditions of power supply voltage and temperature characteristics to determine the worst and best case delay characteristics, rise and fall times". Also see column 2 line 52 "SPICE is a "standard simulator" which has grown into a de-facto industry standard over a number of years.. . HSPICE, and column 4 line 24 "netlist". [Office Action, pages 9-10, sections 54-59].

Applicant respectfully disagrees.

The Office Action seems to be confusing Applicant's "circuit parameter values of a circuit design" with Bair's "simulated conditions of power supply voltage and temperature". This is not consistent with the plain meaning of the claim language. Nor is this consistent with the support that can be found in Applicant's specification.

Clearly, "temperature" cannot be considered part of a circuit design. One or ordinary skill in the art would not consider a reference to a "power supply voltage" to be part of a circuit design of electronic components. Harper-Collins Dictionary of Electronics distinguishes electronic circuits from the power supply in its definition thereof. A "power supply [is] the source of POWER for an electronic circuit that can be AC power, battery, solar cell, or other methods." [Harper-Collins Dictionary of Electronics, Copyright 1991, Page 244, attached hereto as Appendix I].

Moreover, dependent claim 19, 25, 34 clarify what are circuit parameter values of a circuit design by associating them with electronic components: a resistor, capacitor, and inductor.

Clearly resistance, capacitance and inductance cannot be confused as conditions of power supply voltage and temperature.

Moreover as described in Applicant's specification, "the simulation template 400 adds a series of commands (routine) to the netlist to vary each parameter having tolerances associated with it, to run a simulation each time a parameter is varied and store the scalars of the selected vector measurements (i.e. a plot), and to calculate the sensitivity of the vector measurements each time a parameter is varied." [Specification, Page 10, lines 5-8].

Figures 5A-7 and the description in the specification illustrate what exemplary circuit parameters are varied. Figure 5A illustrates resistors R1, R2, R5 and capacitors C3 and C4. In Figure 5B, resistors R1, R2, R5 and capacitors C3 and C4 are the first five elements of the circuit description section 508 of the netlist 500B. In Figure 6-2, resistors R1, R2, R5 and capacitors C3 and C4 have the tolerances (TOL=X%) associated with them in the circuit description section 632 of the netlist 600. "As the built netlist 600 illustrates, circuit description section 632 of the band pass filter has been modified to include tolerance information for the listed parameters. This is the result of the '#tolerance' directive of the sensitivity simulation template 400." [Applicant's Specification, Page 11, lines 6-9].

"Figure 7 illustrates an exemplary output file 700 for the sensitivity analysis performed in accordance with the built netlist 600. For each of the parameters having tolerances, the output file 700 lists the name of the parameter, its nominal value, the scalar (e.g. mean) value the vector (e.g. v(4)) that is being measured, and the sensitivity in percentage of the

selected vector based on the variation of the corresponding parameter. In the example, the sensitivity of mean of voltage v(4) is calculated for variations in resistor r5, resistor r2, capacitor c4, resistor r1, and capacitor c3." [Applicant's Specification, Page 11, line 26 to page 12, line 1]. Figure 7 illustrates the nominal resistances and capacitances associated with resistors R1, R2, R5 and capacitors C3 and C4, respectively, around which they are varied.

"During patent examination, the pending claims must be "given *their broadest reasonable interpretation consistent with the specification." [MPEP § 2111, 8th Ed. Rev 2, May 2004, page 2100-46 citing *In re Hyatt*, 211 F.3d 1367, 1372, 54 USPQ2d 1664, 1667 (Fed. Cir. 2000).] "[D]uring examination the USPTO must give claims their broadest reasonable interpretation. This means that the words of the claim must be given their plain meaning unless applicant has provided a clear definition in the specification." [MPEP § 2111, 8th Ed. Rev 2, May 2004, page 2100-47 citing *In re Zletz*, 893 F.2d 319, 321, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989)]

To construe "altering circuit parameters" as altering power supply voltage and temperature ignores the ordinary meaning of the terms found in the claims and is inconsistent with the meaning of these terms found in the written description of Applicant's disclosure.

Bair does not disclose **altering circuit parameter values** of a circuit design. Bair at Column 3, line 10 only discloses "different simulated conditions of power supply voltage and temperature characteristics" in order to determine basic timing information.

The Office Action tries to support its allegation by citing Bair column 1, line 59 and stating "Bair's 'actual physical characteristics of the device' also discloses the claim 1 term 'circuit parameter'." [Office Action, page 6, Section 34, lines 5-6]. Bair's paragraph beginning at column 1, line 59 is only a general description of a SPICE circuit simulator. However assuming arguendo that a circuit parameter is disclosed in Bair, it still does not disclose **altering circuit parameter values** of a circuit design or adding a routine into a SPICE netlist to do so. (emphasis added).

It is improper to examine Applicant's claims in such a piecemeal fashion as found in the Office Action. "In determining the differences between the prior art and the claims, the question under 35 U.S.C. 103 is not whether the differences themselves would have been obvious, but whether the **claimed invention as a whole** would have been obvious." (emphasis added) [MPEP § 2141.02, 8th Ed., Rev. 2, May 2004, Pages 2100-124 to 2100-125 citing *Stratoflex, Inc. v. Aeroquip Corp.*, 713 F.2d 1530, 218 USPQ 871 (Fed. Cir. 1983)].

For the foregoing reasons, Bair does not disclose "adding a perturbing routine to said SPICE netlist for **altering circuit parameter values of said circuit design** in a pre-determined manner" as recited in claim 1. (emphasis added) [Claim 1, lines 8-9].

As Bair does not disclose **altering circuit parameter values** of a circuit design, it follows that Bair does not disclose "adding a second simulation routine to said SPICE netlist for performing **simulations of said circuit design for respective altered circuit parameter values** to arrive at respective

selected vector measurements" as recited in claim 1. (emphasis added) [Claim 1 as amended, lines 11-14].

Because the **altered circuit parameter values** of the circuit design are used to generate the respective selected vector measurements, <u>Bair</u> also does not disclose "adding an analysis routine to said SPICE netlist for **manipulating at least one of said selected vector measurements** in accordance with said pre-determined analysis" as recited in claim 1. (emphasis added) [Claim 1 as amended, lines 15-18]. <u>Bair</u> at Column 3 line 10 only discloses determining basic timing information, "worst and best case delay characteristics, rise and fall times". Applicant's pre-determined analyses, such as circuit sensitivity analysis for example, require more than a basic timing analysis.

The Office Action admits that "<u>Bair</u> does not expressly disclose "perform[ing] a reference simulation of said SPICE netlist to arrive at nominal values for selected vector measurements". [Office Action, page 10, Sections 60-61]. Instead, the Office Action relies on <u>Chonnad</u> to allegedly disclose this limitation of Applicant's claimed invention in claim 1.

The Office Action alleges that "'perform[ing] a reference simulation of said SPICE netlist to arrive at nominal values for selected vector measurements' is disclosed by <u>Chonnad</u> FIG 1 element 18 "REFERNCE OUTPUT VECTORS", which are also known as "golden output vectors" at column 2 line 18". [Office Action, page 10, section 61, lines 1-4] Applicant respectfully disagrees.

Generally, <u>Chonnad</u> discloses "an improved method for translating between Verilog and VHDL hardware design languages". [<u>Chonnad</u>, Col, 1, lines 9-11]. Specifically in <u>Chonnad</u>'s Figure

1, "a top-level model 14 representing a set of modules which comprise [an] initial RTL-based design 12". [Chonnad, Col. 2, lines 14-15]. However, a register-transfer-level (RTL) based design is not a SPICE netlist. "RTL abstraction describes the functional or behavioral characteristics of a circuit." [Chonnad, Col. 1, lines 19-20]. Moreover, the input test vectors are the binary or digital logic ones and zeros that are coupled into the initial RTL-based design while the output vectors are the binary or digital logic ones and zeros expected to be output from the RTL-based design in response. Test vectors, such as Chonnad's "golden output vectors" are not analog signals or values typically associated with SPICE circuit simulations.

The Office Actions reference to "Nominal Output Vectors" is not disclosed in Chonnad and has no meaning in the context of SPICE circuit simulation. There also is no relation between test vectors (however named) and the definition accepted by the Office Action in section 30. [Office Action, page 5, section 30}.

The Office Action seems to suggest "any changes in the system [of Chonnad]" is the same as Applicant's "[circuit] parameter perturbations". [Office Action, Page 10, Section 61, lines 6-8]. Applicant respectfully disagrees.

Any change in the RTL-based design 12 of Chonnad that effects the outcome of the binary or digital logic ones and zeros that are output is a significant digital logic change and does not disclose the equivalent of a circuit parameter change.

Thus Applicant respectfully submits that Chonnad's REFERENCE OUTPUT VECTORS, a.k.a. "golden output vectors" described at Chonnad's column 2, line 18, do not disclose

"'perform[ing] a reference simulation of said SPICE netlist to arrive at nominal values for selected vector measurements" as is alleged by the Office Action.

As the Office Action admits "'perform[ing] a reference simulation of said SPICE netlist to arrive at nominal values for selected vector measurements" is not disclosed in Bair and as Applicant has shown its also not disclosed by Chonnad, the combination of Bair and Chonnad does not disclose "'perform[ing] a reference simulation of said SPICE netlist to arrive at nominal values for selected vector measurements" as recited in claim 1.

Independent claim 10 has similar elements in comparison with independent claim 1, including *altering circuit parameter values of said circuit design*. Thus, Applicant incorporates here by reference the foregoing remarks with respect to independent claim 1 to put independent claim 10 in condition for allowance.

"To establish a prima facie case of obviousness, … the prior art reference (or references when combined) must teach or suggest all the claim limitations." [MPEP § 2142; 8th Edition, Rev. 1, Feb. 2003, Pg. 2100-124, citing In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)]. Applicant respectfully submits that the combination of Bair and Chonnad does not disclose all the claim limitations found in independent claims 1 and 10.

Thus for the foregoing reasons, Applicant respectfully submits that independent claims 1, and 10 are not made obvious by the combination of Bair and Chonnad.

Regarding independent claim 31 rejected over the
combination of <u>Bair</u>, <u>Chonnad</u> and <u>Tucker</u>, the Office Action
alleges:

"limitation (a), "providing a SPICE netlist of a circuit
design" is disclosed by <u>Bair</u> at column 2 line 52 "SPICE is a
"standard simulator" which has grown into a de-facto industry
standard over a number of years.. . HSPICE", and column 4 line
24 "netlist".

limitation (b), "selecting a selected vector measurement of
the circuit design" is disclosed by <u>Bair</u> at Column 3 line 10
"The circuit-level simulation is run under several different
simulated conditions of power supply voltage and temperature
characteristics to determine the worst and best case delay
characteristics, rise and fall times". Also see column 2 line 52
"SPICE is a "standard simulator" which has grown into a de-facto
industry standard over a number of years.. . HSPICE", and column
4 line 24 "netlist".

limitation (d), "altering at least one circuit parameter
value of a component in the SPICE netlist in a pre-determined
manner to generate at least one altered circuit parameter value"
is disclosed by <u>Bair</u> at Column 3 line 10 "The circuit-level
simulation is run under several different simulated conditions
of power supply voltage and temperature characteristics to
determine the worst and best case delay characteristics, rise
and fall times".

limitation (e), "simulating the SPICE netlist of the
circuit design with the at least one altered circuit parameter
value to determine an altered vector measurement
associated with the selected vector measurement" is disclosed by
<u>Bair</u> at Column 3 line 10 "The circuit-level simulation is run

under several different simulated conditions of power supply
voltage and temperature characteristics to determine the worst
and best case delay characteristics, rise and fall times".

limitation (f), "repeating steps (d) and (e) with the at
least one circuit parameter value to generate a plurality of
altered circuit parameter value to generate a plurality of
altered circuit parameter values an to determine a plurality of
altered vector measurements of the circuit design" is disclosed
by Bair at Column 3 line 10 "The circuit-level simulation is run
under several different simulated conditions of power supply
voltage and temperature characteristics to determine the worst
and best case delay characteristics, rise and fall times".

"limitation (c), "simulating the SPICE netlist of the
circuit design using nominal circuit values to determine a
nominal vector measurement associated with the selected vector
measurement" is Chonnad FIG 1 element 18 "REFERENCE OUTPUT
VECTORS", which are also known as "golden output vectors" at
column 2 line 98. In other words, a base set of input vectors is
used to generate a base set of output vectors (reference output
vectors, or golden output vectors, or nominal output vectors)
for the base system. Any changes in the system ("parameter
perturbations" in the Applicant's terminology) are evaluated by
comparison of the new output vectors against the reference
output vectors"; and

"limitation (g), "determining a difference between the
plurality of altered vector measurements and the nominal vector
measurement to generate a sensitivity in the vector measurement
of the circuit design in response to alterations in the at least
one circuit parameter value of the component in the SPICE
netlist" is disclosed by Tucker at Page 862 "Sensitivity

analysis refers to methods of calculating the rates of change of
: (1) response quantities.. .(2) optimum design variable
values"."

Applicant respectfully disagrees.

Independent claim 31 includes the limitation of "(d)
altering at least one **circuit parameter value** of a component in
the SPICE netlist in a pre-determined manner to generate at
least one altered circuit parameter value". [Claim 31, lines
10-12]. This is somewhat similar to the limitation of "altering
circuit parameter values of said circuit design" found in
independent claims 1 and 10. Thus, Applicant incorporates here
by reference the foregoing remarks with respect to independent
claim 1.

It is clear from the plain language of the claim that
Applicant's limitation is directed to "altering at least one
circuit parameter value *of a component in the SPICE netlist*" and
not a power supply voltage or a temperature. (emphasis added)

For this reason and the foregoing reasons found in the
remarks of claim 1, Applicant respectfully submits that Bair
does not disclose "(d) altering at least one circuit parameter
value of a component in the SPICE netlist in a pre-determined
manner to generate at least one altered circuit parameter value;
(e) simulating the SPICE netlist of the circuit design with the
at least one altered circuit parameter value to determine an
altered vector measurement associated with the selected vector
measurement; [and] (f) repeating steps (d) and (e) with the at
least one circuit parameter value to generate a plurality of
altered circuit parameter values and to determine a plurality of
altered vector measurements of the circuit design" as is recited

in claim 31. [Claim 31, lines 10-20]. Nor does <u>Chonnad</u> or

<u>Tucker</u> disclose these limitations recited in Applicants claim

31.

The Office Action admits that <u>Bair</u> does not disclose the

limitations of element (c). [Office Action, page 16, section

96]. Instead, the Office Action uses <u>Chonnad</u> to allege

"simulating the SPICE netlist of the circuit design using

nominal circuit values to determine a nominal vector measurement

associated with the selected vector measurement" is [disclosed

by] <u>Chonnad</u> FIG 1 element 18 "REFERENCE OUTPUT VECTORS", which

are also known as "golden output vectors" at column 2 line 98."

[Office Action, page 16, section 97]. Applicant respectfully

disagrees.

The allegation raised in section 97 of the Office Action is

substantially similar to the allegation raised in section 61.

Applicant incorporates here by reference its remarks with

respect to <u>Chonnad</u> previously made in placing independent claim

1 in condition for allowance.

Thus, Applicant respectfully submits that <u>Chonnad</u>'s

REFERENCE OUTPUT VECTORS, a.k.a. "golden output vectors"

described at <u>Chonnad</u>'s column 2, line 18, do not disclose

"simulating the SPICE netlist of the circuit design using

nominal circuit values to determine a nominal vector measurement

associated with the selected vector measurement" as is alleged

by the Office Action. Nor does <u>Tucker</u> disclose "(c) simulating

the SPICE netlist of the circuit design using nominal circuit

parameter values to determine a nominal vector measurement

associated with the selected vector measurement" as is recited

in Claim 31. [Claim 31, lines 6-9].

The Office Action admits that <u>Bair</u> does not disclose the limitations of element (g). [Office Action, page 16, section 96]. Instead, the Office Action uses <u>Tucker</u> to allege "determining a difference between the plurality of altered vector measurements and the nominal vector measurement to generate a sensitivity in the vector measurement of the circuit design in response to alterations in the at least one circuit parameter value of the component in the SPICE netlist" is disclosed by <u>Tucker</u> at Page 862 "Sensitivity analysis refers to methods of calculating the rates of change of : (1) response quantities...(2) optimum design variable values". Applicant respectfully disagrees.

While <u>Tucker</u> generally discloses that sensitivity analysis is known, <u>Tucker</u> does not disclose a sensitivity analysis in a "vector measurement of [a] circuit design in response to alterations in the at least one circuit parameter value of the component in the SPICE netlist" as recited in Applicant's independent claim 31. [Claim 31, lines 23-26]. Nor does <u>Chonnad</u> disclose a sensitivity analysis in a "vector measurement of [a] circuit design in response to alterations in the at least one circuit parameter value of the component in the SPICE netlist" as recited in Applicant's independent claim 31. [Claim 31, lines 23-26].

"To establish a prima facie case of obviousness, … the prior art reference (or references when combined) must teach or suggest all the claim limitations." [MPEP § 2142; 8th Edition, Rev. 1, Feb. 2003, Pg. 2100-124, citing In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)]. Applicant respectfully submits that the combination of <u>Bair</u>, <u>Chonnad</u>, and <u>Tucker</u> does not disclose all the claim limitations.

Thus for the foregoing reasons, Applicant respectfully submits that independent claim 31 is not made obvious by the combination of <u>Bair</u>, <u>Chonnad</u>, and <u>Tucker</u>.

Regarding dependent claim 2, the Office Action alleges that "adding tolerances" is disclosed by <u>Bair</u> at Column 3 line 12 "determine the worst and best case delay characteristics, rise and fall times." [Office Action, page 11, section 64}. Applicant respectfully disagrees.

Here again the Office Action seems to be improperly taking a limitation out of context and ignoring the claim as a whole. Claim 2 recites the limitation of "adding tolerances in a SPICE netlist for said circuit parameters".

As discussed previously, an example of adding tolerances to circuit parameters is illustrated by Applicant's Figure 6-2. In Applicant's Figure 6-2, resistors R1, R2, R5 and capacitors C3 and C4 have tolerances (TOL=X%) associated with them in the circuit description section 632 of the netlist 600. As described in Applicants Specification, "the built netlist 600 illustrates, circuit description section 632 of the band pass filter has been modified to include tolerance information for the listed parameters. This is the result of the '#tolerance' directive of the sensitivity simulation template 400." [Applicant's Specification, Page 11, lines 6-9].

<u>Bair's</u> disclosure at Column 3 line 12 of the worst and best case delay characteristics, rise and fall times is disclosing basic timing information for an output of a circuit in response to an input stimulus. It does not disclose adding anything to a netlist. More specifically, <u>it</u> does not disclose "**adding tolerances** in the netlist *for [the] circuit parameter values*" as

recited in claim 2. (emphasis added) The different simulated conditions for power supply voltage and temperature to determine worst and best case delay characteristics, rise and fall times in Bair also does not disclose adding tolerances to circuit parameter values in a netlist.

The Office Action tries to support its allegation by citing Bair column 1, line 59 and stating "Bair's 'actual physical characteristics of the device' also discloses the claim 1 term 'circuit parameter'." [Office Action, page 6, Section 34, lines 5-6].

Bair's paragraph beginning at column 1, line 59 is only a general description of a SPICE circuit simulator and a transistor model. However assuming arguendo that a circuit parameter is disclosed in Bair, Bair does not disclose **altering** the circuit parameter value of a circuit design, nor adding a routine into a SPICE netlist to do so. (emphasis added).

Neither Chonnad nor Tucker disclose adding tolerances to circuit parameter values in a netlist as recited in the claim.

Thus for the foregoing reasons, Applicant respectfully submits that claim 2 is not made obvious by the cited combination of Bair and Chonnad, with or without Tucker.

Regarding dependent claim 6, the Office Action alleges that a ""pre-determined analysis includes a sensitivity analysis involving a difference between said respective selected vector measurements and said nominal values for said selected vector measurements" is disclosed by Tucker at Page 862 "Sensitivity analysis refers to methods of calculating the rates of change of: (1) response quantities.. .(2) optimum design variable

values". [Office Action, page 11, section 67. Applicant respectfully disagrees.

While Tucker generally discloses that sensitivity analysis is known, Tucker does not disclose a sensitivity analysis that is performed using selected vector measurements on a SPICE netlist of a circuit design. As described in Applicant's specification, a vector measurement can be "for example, a voltage at a particular node, a current along a particular path, and/or the power dissipation across a particular component". [Applicant's specification, page 7, lines 1-2]. Applicant's vector measurements are generated by performing simulations of a circuit design as recited in independent claim 1. Thus, Tucker does not disclose "a sensitivity analysis involving determining a difference between said respective selected vector measurements and said nominal values for said selected vector measurements" as recited in amended claim 6. [Claim 6, lines 4-7]. Nor does Chonnad disclose a sensitivity analysis using selected vector measurements on a SPICE netlist of a circuit design.

Regarding dependent claim 8, the Office Action alleges that an "extreme value analysis" is disclosed by Bair at Column 3 line 11 "different simulated conditions … best and worst case". [Office Action, page 11, section 69, lines 1-2]. Applicant respectfully disagrees.

As discussed previously, Bair at Col. 3, lines 10-13 does not disclose altering circuit parameter values, only power supply voltage and temperature. Bair does not disclose "circuit parameter values at their extreme tolerance values" as recited in claim 8. [Claim 8, lines 7-8]. Without "circuit parameter

values at their extreme tolerance values", <u>Bair</u> does not disclose "an extreme value analysis involving a determination of a maximum of said difference between said respective selected vector measurements and said nominal values for said selected vector measurements" as recited in claim 8. [Claim 8, lines 3-6].

Regarding dependent claim 9, the Office Action alleges that "a worst case by sensitivity analysis involving a maximum of an absolute value of said difference between said respective selected vector measurements and said nominal selected vector measurements" is disclosed by <u>Bair</u> at Column 3 line 5 "simulation results which will give best indication of the delay characteristics" and Column 3 line 12 "determine worst and best case". [Office Action, pages 11-12, section 70, lines 1-5}. Applicant respectfully disagrees.

As discussed previously with respect to independent claim 1, <u>Bair</u> does not disclose ***altered circuit parameter values*** of the circuit design being used to generate the respective selected vector measurements. <u>Bair</u> at Column 3 line 12 only discloses determining basic timing information, "worst and best case delay characteristics, rise and fall times", and the input stimulus (i.e., "what stimuli") to do so at <u>Bair</u>'s Column 3, line 5. That is, <u>Bair</u> does not disclose "a worst case by sensitivity analysis involving a maximum of an absolute value of said difference between said respective selected vector measurements and said nominal values for said selected vector measurements" as recited in claim 9. [Claim 9 as amended, lines 3-5].

Regarding dependent claims 19-23 and 34-35, the Office Action alleges that Applicant's circuit parameter values, selected vector measurements, and components of said circuit design are implicitly disclosed by Bair at column 4, line 24 by "netlist" and/or column 1, line 60 "circuit elements … voltages and currents". [Office Action, pages 12-13 and 17, sections 77-81, 104-105] Applicant respectfully disagrees.

Bair at column 4, line 24 defines a "netlist is a file comprising descriptions of the logic primitives (e.g., AND/OR gates, etc.) used in the logic schematic and the interconnections therebetween." [Bair, Col. 4, lines 24-27]. Bair discloses using logic primitives in its netlist and not circuit components of a SPICE netlist. This may implicitly disclose determining logic functionality (i.e., binary or digital logic ones and zeroes) but not circuit measurements of voltages, currents, and power dissipation.

At column 1, line 64 of Bair, it states "Voltages and currents are modeled as continuously variable entities, rather than the simple one-zero modeling of digital simulators." [Bair, column 1, lines 64-66]. In Bair, this seems to be in reference to modeling input currents and voltages, as it says nothing about taking measurements in a netlist.

Regarding dependent claims 24 and 36, the Office Action alleges that "only one circuit parameter value of said circuit design is altered at a time by the perturbing routine" and "only one circuit parameter value of said circuit design is altered at a time" is disclosed by Tucker at Page 862 "Sensitivity analysis refers to methods of calculating the rates of change of: (1) response quantities.. .(2) optimum design variable values".

[Office Action, page 14, section 85, lines 1-4]. Applicant respectfully disagrees.

While <u>Tucker</u> generally discloses that sensitivity analysis is known, <u>Tucker</u> does not disclose a sensitivity analysis with regard to **only one circuit parameter value** of a circuit design. (emphasis added).

Regarding dependent claims 32-33 and 38-39, the Office Action improperly alleges over and over again that the same cited reference discloses every limitation in the claims without explanation, when it does not. As is cited by the Office Action, <u>Bair</u> at column 3 line 10 only discloses a "circuit-level simulation is run under several different simulated conditions of power supply voltage and temperature characteristics to determine the worst and best case delay characteristics, rise and fall times". This does not disclose the limitations found in Applicant's claims 32-33 and 38-39.

For example, dependent claim 32 recites "a simulation template is used to perform steps (b)-(g)". Applicant's "Figure 3 illustrates a flow diagram of a simulation template 300 used to build a netlist that performs a sensitivity analysis on the proposed circuit design." [Specification, page 7, lines 30-31]. Applicant's "Figure 4 illustrates in more detail a preferred implementation of an ICL script of a simulation template 400 that builds a netlist to perform a sensitivity analysis." [Specification, page 9, lines 3-4].

Applicant's Summary of the Invention section describes "a simulation template which is used to modify a netlist that describes the circuit in order to provide customized or pre-installed analysis beyond the analysis available in standard

SPICE. More specifically, a simulation template is an interactive command language (ICL) script that has embedded instructions telling a netlist where to insert information and which options are to be provided. It is used to expand SPICE beyond the traditional limitations of the basic alternating current (AC), direct current (DC), and transient analysis by allowing parameter variations and multiple simulations passes to be run under one analysis umbrella." [Specification, page 3, lines 11-18]. With this in mind, Bair clearly does not disclose "a simulation template [is used] to perform steps (b)-(g) of claim 31.

However, the Office Action seems to improperly ignore the plain meaning of the claim language and the support provided by the specification in these claim rejections. Additionally, it is improper to use a hindsight analysis of the claims.

Moreover, rejected claims 2-3, 6, 8-9, and 19-23 are dependent from independent claim 1. Applicant believes that independent claim 1 has been placed in condition for allowance such that dependent claims depending there from are also in condition for allowance.

Rejected dependent claims 11-12, 15, and 17-18 are dependent from independent claim 10 and have similar elements as found in dependent claims 2-3, 6, and 8-9, respectively. Applicant believes that independent claim 10 has been placed in condition for allowance such that dependent claims depending there from are also in condition for allowance.

Rejected dependent claims 32-36 and 38-39 are dependent from independent claim 31. Applicant believes that independent claim 31 has been placed in condition for allowance such that

dependent claims depending there from are also in condition for allowance.

B. Improper to Combine Bair and Chonnad

Moreover, Bair teaches away from using test vectors, such as Chonnad's "golden output vectors", in SPICE circuit simulators. As stated by Bair, in a SPICE circuit simulator "Voltages and currents are modeled as continuously variable entities, rather than the simple one-zero modeling of digital simulators." [Bair, Col. 2, lines 1-3].

"It is improper to combine references where the references teach away from their combination." [MPEP §2145(X.D.2), 8th Edition, Rev. 2, May 2004, Pg. 2100-162; citing In re Grasselli, 713 F.2d 731, 743, 218 USPQ 769, 779 (Fed. Cir. 1983)] "A prior art reference must be considered in its entirety, i.e., as a whole, including portions that would lead away from the claimed invention." [MPEP §2141.02, 8th Edition, Rev. 2, May 2004, Pg. 2100-127; citing W.L. Gore & Associates, Inc. v. Garlock, Inc., 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983), cert. denied, 469 U.S. 851 (1984)].

C. Legal Precedent (eliminating element)

The Office Action relies on the legal precedent of "eliminating element" in rejecting claims 3 and 12.

In section 39, the Office Action alleges that "Applicant distinguished the facts of Ex Parte Wu from claim 1 by asserting that Ex Parte Wu is limited to methods of decreasing corrosion rate in the chemical and material science arts, and does not apply to the instant claims of regarding software simulation of circuits." [Office Action, page 7, section 39].

It seems that Applicant's prior response may not have been completely considered by the Office Action and is repeated herein with emphasis added.

"As discussed in MPEP § 2144, if the facts in a prior legal decision are sufficiently similar to those in an application under examination, the examiner may use the rationale used by the court." [MPEP § 2144.04, 8th Edition, Rev.2, May 2004; page 2100-138].

The cited legal precedent for omission of an element and its function in the MPEP 2144.04(II.A.) is *Ex parte Wu*, 10 USPQ 2031 (Bd. Pat. App. & Inter. 1989). A copy of the decision in Ex Parte Wu is attached hereto as Exhibit I for the Examiner's reference as MPEP 2144.04(II) paraphrases the case and the decision.

The claims and application in *Ex parte Wu* were "directed to a process for using a particular composition to inhibit corrosion on a metal surface." [*Ex parte Wu*, 10 USPQ 2031 at 2032 (Bd. Pat. App. & Inter. 1989)]. **Patentability in *Ex parte Wu* turned on the material composition and the claim language "consisting of" that excluded other elements from being a part of the claimed material composition.** (emphasis added) **The**

material composition of the prior art reference in *Ex parte Wu* disclosed all of the elements of the claimed material composition but with additional elements. (emphasis added) **The court found that omitting the additional elements in the material composition of the prior art reference was obvious.** (emphasis added)

The *Ex parte Wu* claims recite a "method of decreasing corrosion rate by contacting a metal surface with a material composition consisting of" in the chemical or material science arts and not a computer readable medium or a method of modifying a SPICE netlist for a software simulator in the general field of computer programming.

Moreover, **Applicant's claims 3 and 12 do not recite the limitation "consisting of" in order to exclude other elements from a set of elements.** (emphasis added) **Applicant's claims 3 and 12 recite an additional step** of "removing parameter and vector save statements in said SPICE netlist". (emphasis added) [Claims 3, 12 as amended, lines 2-3]. This conserves "memory space since a vector measurement may comprise large amounts of data, which would require a substantial memory size if numerous simulations are performed in the simulation template analysis." [Specification, page 8, lines 7-9].

Additionally, **the Office Action does not properly apply the legal precedent to exclude an element found in the prior art reference of Bair.** (emphasis added) **In *Ex Parte Wu*, an element found in the material composition of the prior art reference was excluded in order to make the claims obvious.** (emphasis added) The Office Action admits that **Bair "does not expressly disclose the additional limitation."** [Final Office Action, page 9, section 66, line 1]. **As Bair does not disclose an additional**

**limitation that is supposed to be excluded by Applicant's
claims, there is no reason to apply the legal precedent set
forth by *Ex Parte Wu*.** (emphasis added).

The Office Action further states that "Applicant does not
assert that the element is eliminated while the function is
retained, which would be indicia of nonobviousness per MPEP
2144.04(II.B)." [Office Action, Page 7, Section 40}. This is
because Applicant's claims 3 and 12 add an element and are not
excluding other elements. The Office Action has failed to find
Applicant's additional limitation in a prior art reference.

Applicant respectfully submits that the facts of *Ex parte
Wu* are not sufficiently similar to the facts in Applicant's
patent application and Applicant's claims.

For the foregoing reasons, Applicant respectfully submits
that the Examiner cannot rely on the legal precedent
(eliminating element) of *Ex parte Wu* to reject Applicant's
claims 3 and 12.

D. Conclusion

Thus for all of the foregoing reasons, Applicant
respectfully submits that the cited combinations of references
and legal precedents do not make Applicant's claims 1-3, 6, 8-
12, 15, 17-36, and 38-39 obvious under 35 USC § 103(a).

Accordingly, Applicant respectfully requests the withdrawal
of all the 35 USC § 103(a) claim rejections of claims 1-3, 6, 8-
12, 15, 17-36, and 38-39.

V.   New Claims

Applicant has added new claims 40-48 by this response.

New claims 40-42 are dependent claims depending directly or indirectly from independent claim 1.

New claims 43-45 are dependent claims depending directly or indirectly from independent claim 10.

New claims 46-48 are dependent claims depending directly or indirectly from independent claim 31.

As discussed previously, Applicant believes that it has placed independent claims 1, 10, and 31 in condition for allowance such that dependent claims 40-42, 43-45, and 46-48 depending respectfully there from with added limitations are also in condition for allowance.
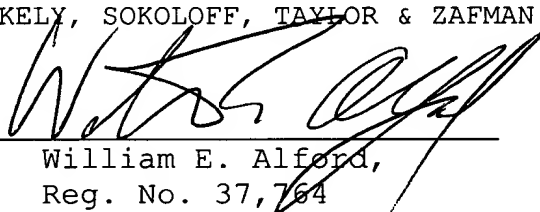
CONCLUSION

In view of the foregoing it is respectfully submitted that the pending claims are in condition for allowance. Reconsideration is requested. Allowance of the claims at an early date is solicited.

The Examiner is invited to contact Applicant's undersigned counsel by telephone at (714) 557-3800 to expedite the prosecution of this case should there be any unresolved matters remaining. Please charge any shortage in fees in connection with the filing of this paper to Deposit Account 02-2666 and please credit any excess fees to such deposit account.

Respectfully submitted,

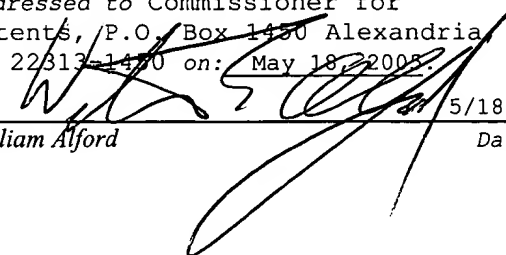BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: May 18, 2005

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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to Commissioner for Patents, P.O. Box 1450 Alexandria, VA 22313-1450 on: May 18, 2005.

William Alford   5/18/05
                                  Date